IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Jin-Hyuk LEE, et al.		
Serial No.:	10/690,782	Examiner:	Graybill, David E.
Filed:	October 21, 2003	Group Art Unit:	2822
Confirmation No.:	5611		
For:	METHOD FOR MANUFACTURING A WAFER LEVEL CHIP SCALE PACKAGE		
Date:	September 5, 2006		

Mail Stop Amendment
Commissioner for Patents
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AMENDMENT

Responsive to the Office Action, Paper No. 20060608, dated June 14, 2006, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

IN THE CLAIMS

1. (Currently amended) A method for a wafer level chip scale package (CSP), the method comprising:

providing a semiconductor wafer, the semiconductor wafer including semiconductor chips having chip pads and a passivation layer, the wafer further including scribe lines between the chips;

forming a first patterned dielectric layer on the passivation layer that exposes the chip pads;

forming a second patterned dielectric layer on the first patterned dielectric layer that exposes the chip pads;

forming an embossed ~~portion~~ region on the first patterned dielectric layer, the second patterned dielectric layer, and the passivation layer including a concave portion that exposes a portion of the ~~first patterned dielectric~~ passivation layer where a ball pad is to be formed and a convex portion that is formed from the second patterned dielectric layer;

forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, ~~and~~ the exposed portion of the second patterned dielectric layer[[s]], and the exposed portion of the passivation layer ~~including the embossed portion~~, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer over the embossed ~~portion~~ region to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer to form the ball pad.

2. (Cancelled)

3. (Currently amended) The method of claim 1, wherein the concave portion comprises a ~~circle~~ substantially cylindrical shape and the convex portion has an annular shape.

4. (Currently amended) The method of claim 1, wherein the convex portion comprises a single discontinuous ring shape.

5. (Previously presented) The method of claim 1, wherein an area of the concave portion is inside the convex portion.

6. (Cancelled)

7. (Previously presented) The method of claim 1, further comprising:

forming a solder ball on the ball pad; and

cutting the semiconductor wafer along the scribe lines.

8. (Cancelled)

9. (Previously presented) The method of claim 3, wherein forming a second patterned dielectric layer comprises exposing a portion of the first patterned dielectric layer inside the annular convex portion.

10. (Currently amended) A method for a wafer level chip scale package (CSP) comprising:

providing a semiconductor wafer, the semiconductor wafer including semiconductor chips each having chip pads and a passivation layer;

forming a first dielectric layer on the passivation layer;

patterning the first dielectric layer to expose the chip pads;

forming a second dielectric layer on the patterned first dielectric layer;

patterning the second dielectric layer to expose the chip pads;

forming an embossed ~~portion~~ region on the first patterned dielectric layer, the second patterned dielectric layer, and the passivation layer;

forming a concave portion in the embossed ~~portion~~ region that includes an exposed portion of the ~~first dielectric~~ passivation layer where a ball pad is to be formed;

forming a convex portion in the embossed ~~portion~~ region ~~of the second dielectric layer~~;

forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, ~~and~~ the exposed portion of the second patterned dielectric

layer[[s]], and the exposed portion of the passivation layer, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer over the embossed ~~portion~~ region to form a ball pad.

11. (Cancelled)

12. (Previously presented) The method of claim 10, further comprising:

forming a solder ball on the ball pad.

13. (Withdrawn) A wafer level chip scale package (CSP), comprising:

a semiconductor chip having chip pads and a passivation layer exposing chip pads;

a first patterned dielectric layer disposed on the passivation layer; and

a second patterned dielectric layer, the first and second patterned dielectric layers exposing the chip pads,

wherein the first and second patterned dielectric layers have an embossed portion comprising a concave portion and a convex portion, the concave portion exposing a portion of the first patterned dielectric layer where a ball pad is to be formed, the convex portion being formed of the second patterned dielectric layer.

14. (Withdrawn) The apparatus of claim 13, wherein the concave portion comprises a circle shape, and the convex portion comprises a ring shape and having a smaller diameter than the concave portion.

15. (Withdrawn) The apparatus of claim 13, wherein the convex portion comprises a discontinuous ring shape.

16. (Withdrawn) The apparatus of claim 13, wherein the area of the concave portion inside the convex portion is approximately equal to the area of the convex portion.

17. (Currently amended) A method of making a wafer level chip scale package (CSP), the method comprising:

providing a semiconductor wafer, the semiconductor wafer including a semiconductor chip having chip pads and a passivation layer, the wafer further including scribe lines between the chips;

forming a first patterned dielectric layer on the passivation layer that exposes the chip pads;

forming a second patterned dielectric layer on the first patterned dielectric layer that exposes the chip pads, wherein the first patterned dielectric layer, ~~and~~ the second patterned dielectric layer[[s]], and the passivation layer have an embossed ~~portion~~ region comprising a[[n]] ~~annular~~ substantially cylindrical concave portion and an annular convex portion, the concave portion exposing a portion of the ~~first patterned dielectric~~ passivation layer where a ball pad is to be formed, the convex portion being formed of the second dielectric layer;

forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, ~~and~~ the exposed portion of the second patterned dielectric layer[[s]], and the exposed portion of the passivation layer, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer to form a connection hole that exposes a portion of the metal wiring layer.

18. (Previously presented) The method of claim 3 wherein the convex portion is contained within the concave portion.

19. (Currently amended) The method of claim 18 wherein the convex portion is bounded by substantially vertical side walls and wherein said method further includes forming a ball pad on the concave portion, the convex portion, and the walls.

20. (Cancelled)

21. (Previously presented) The method of claim 5 wherein the area of the concave portion inside the convex portion is approximately equal to an area of the convex portion.

REMARKS

Claims 1, 3-5, 7, 9, 10 and 12-21 are pending in the application.

Claims 13-16 are withdrawn from consideration.

Claims 1, 3-5, 7, 9, 10, 12 and 17-21 are rejected.

Claims 1, 3, 4, 7, 10, 12 and 17-19 are rejected under 35 U.S.C. 103(a).

Claims 3, 4, 5, 9, 17 and 21 are rejected under 35 U.S.C. 103(a).

Claim 20 is rejected under 35 U.S.C. 103(a).

Claims 1, 3, 4, 10, 17 and 19 have been amended.

Claim 20 has been cancelled.

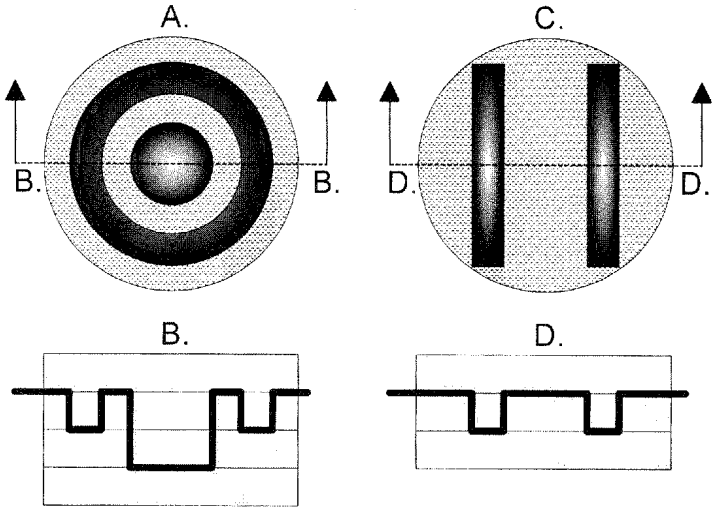
No new matter has been added.

Claims 1, 3-5, 7, 9, 10, 12, 17-19 and 21 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and the following remarks.

Rejection Regarding Purpose and Result

The Applicant traverses the Examiner's characterization that the shapes set forth in the present application, which substantially increase the contact area of the ball with the metal over those shapes known in the prior art, are mere dimensions without a purpose. The Examiner goes so far as to say that they lack **any** purpose or produce **any** result. O.A. page 7. The Applicant provides a demonstrable example to the contrary in the following Figures A., B., C. and D.



Exemplary Figures A. and B., which is a cross-sectional view taken along line B-B in Figure A, are similar to the present application Figures 19 and 18 respectively. Figures C. and D., which is a cross-sectional view taken along line D-D in Figure C, correspond with the disclosure in Cho (6,400,021)—one of the primary references cited by the Examiner. *See, e.g.,* Col. 4, Lines 13-18, and Fig. 14.

The Applicant notes that the exemplary embodiment shown in Figures A. and B. teaches a substantial improvement over the prior art shown in Figures C. and D. The total surface area formed in the region shown in Figures A. and B. covers a substantially cylindrical concave portion—multiple dielectric layers deep—and an annular convex portion that together or alone provide substantially more surface area than any reference cited by the Examiner. This results, as taught in the present application, in a contact area between a solder ball and a metal wiring layer that is significantly increased thereby improving the connection reliability between the ball pad and the solder ball. In contrast, the prior art shown in Figures C. and D., as in Cho, teaches "grooves" that form an "uneven shape" etched out of a single dielectric layer. *See, e.g.,* Col. 4, Lines 13-18 and 57-67, and Fig. 14. The other references cited by the Examiner teach ball pads with even less surface area. For example, Yamaguchi (6,780,748) teaches a flat ball pad. *See* Fig. 16. Peng (6,444,295) teaches a "top metal layer" with an "irregular" pattern. *See* Fig. 2(a) and Abstract. Yunus ((2003/0234447) teaches a "castellated contour" characterized by a "groove." *See* Para. 0057. Simply stated, the prior art does not teach the improved methods of forming ball pads with significantly more surface area and greater reliability as taught in the present application. Thus, reconsideration of this rejection is requested, especially in view of the following amendments to the independent claims.

Claim Rejections - 35 U.S.C. 103

Claims 1, 3, 4, 7, 10, 12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (6,780,748) and Cho (6,400,021). The applicant respectfully traverses the rejection.

Claims 1, 3, 4, 7, 10, 12 and 17-19 stand rejected under § 103 as obvious over Yamaguchi in view of Cho. Claims 1 and 10 have been amended to recite: providing . . . chip pads and a passivation layer; forming a first dielectric layer on the passivation layer; . . . forming a second dielectric layer on the patterned first dielectric layer; . . . forming an embossed region

on the first patterned dielectric layer, the second patterned dielectric layer, and the passivation layer; . . . forming a concave portion . . . that exposes a portion of the passivation layer; . . . forming a convex portion in the embossed region; . . . forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, the exposed portion of the second patterned dielectric layer, and the exposed portion of the passivation layer, the metal wiring layer being electrically connected to the chip pads; forming a third dielectric layer on the metal wiring layer; and removing a portion of the third dielectric layer to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer. . . . The amendments are supported by the present application. *See* e.g., Page 8, Lines 26-34, Page 9, Lines 1-24, and FIG. 18-21.

In contrast, Yamaguchi and Cho fail to teach each and every limitation of the amended claims whether individually or in combination with one another. For example, Yamaguchi teaches how to form a metal wiring layer on an "adhesion layer" made of "[c]hromium, titanium, tungsten or the like." Col. 9, Lines 24-39 and FIG. 15. As a result, Yamaguchi does not teach forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, the exposed portion of the second patterned dielectric layer, and the exposed portion of the passivation layer. Further, Yamaguchi does not teach any of the limitations involving an embossed region including concave and convex portions formed on the first and second dielectric layers, much less on the passivation layer.

Similarly, Cho fails to teach forming a metal wiring layer as recited in the claims. For example, Cho teaches forming a metal layer "deposited on the lower dielectric layer." Col. 4, Lines 19-20. Thus, Cho does not teach forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, the exposed portion of the second patterned dielectric layer, and the exposed portion of the passivation layer.

Furthermore, Cho does not teach a first dielectric layer, a second dielectric layer, a third dielectric layer, and a passivation layer. Cho teaches a protection layer 20, a lower dielectric layer 30, and an upper dielectric 50. *See* FIG. 9-14, Col. 4, Lines 4-56. As a result, Cho also fails to teach the embossed region as recited in the claims. For example, Cho teaches the "right portion of the lower dielectric layer 30 on which a solder ball 60 is to be loaded later, is etched to form at least two grooves 32." Cho further teaches that the "upper dielectric layer applied on the grooves is selectively etched, so as to form a ball land 51," the ball land being substantially flat

according to the figures. *See* FIGS. 7-14 and Col. 4, Lines 57-59. If together the substantially flat ball land and grooves cited by the Examiner is the embossed region in the recited claims, then the embossed region is not formed on a first patterned dielectric layer, a second patterned dielectric layer, and a passivation layer as recited in claims 1 and 10. Further, if the grooves are the concave portion of the embossed region, then the concave portion does not include an exposed portion of a passivation layer also as recited in claims 1 and 10. In other words, the concave portion of Cho is one dielectric layer deep, and lacks the substantial additional surface area provided by forming a concave portion in the embossed region that includes an exposed portion of the passivation layer.

As taught by the present claims, the contact area between the solder ball and the metal wiring layer can be significantly increased over the prior art. Thus, claims 1 and 10 are in proper form for allowance. Claim 7 depends from claim 1, and is also in proper form for allowance based at least on its dependency from claim 1. Claim 12 depends from claim 10, and is also in proper form for allowance based at least on its dependency from claim 10.

Claims 3, 4, 5, 9, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi and Cho as applied to claims 3 and 17 supra, and further in combination with Peng (6,444,295). The applicant respectfully traverses the rejection.

Claims 3, 4, 5, 9, 17 and 21 stand rejected under § 103 as obvious over Yamaguchi in view of Cho and Peng. Claim 17 has been amended to recite wherein the first patterned dielectric layer, the second patterned dielectric layer, and the passivation layer have an embossed region comprising a substantially cylindrical concave portion and an annular convex portion, the concave portion exposing a portion of the passivation layer where a ball pad is to be formed, the convex portion being formed of the second dielectric layer; forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, the exposed portion of the second patterned dielectric layer, and the exposed portion of the passivation layer, the metal wiring layer being electrically connected to the chip pads; forming a third dielectric layer on the metal wiring layer; and removing a portion of the third dielectric layer to form a connection hole that exposes a portion of the metal wiring layer.

In contrast, Yamaguchi, Cho, and Peng fail to teach each and every limitation of the amended claim whether individually or in combination with one another. As discussed supra, Yamaguchi fails to teach an embossed region including concave and convex portions. Cho

teaches a concave portion. However, Cho's concave portion consists of "grooves" that form an "uneven shape." *See* Col. 4, Lines 17-18 and 65-67. Thus, if the grooves that form an uneven shape referenced in Cho is the concave portion recited in amended claim 17, the concave portion is not substantially cylindrical. More specifically, claim 17 teaches an annular convex portion in addition to the cylindrical concave portion. An annular shape has more surface area than a groove shape when bounded by similar geometric constrained areas where formation of a solder ball land is desired. The grooves taught by the prior art have less surface area than the substantially cylindrical concave portion and the annular convex portion of the embossed region of claim 17. Admittedly, Peng teaches "[p]atterns composed with a plurality of concentric rings." Col. 4, Line 12. But if Peng's plurality of concentric rings is the concave portion, the concave portion is not substantially cylindrical as recited in amended claim 17. Thus, the applicant submits that claim 17 is in proper form for allowance.

Claim 3 has been amended to recite wherein the concave portion comprises a substantially cylindrical shape and the convex portion has an annular shape. Thus, for reasons similar to those of amended claim 17 noted above, claim 3 is in proper form for allowance.

Claim 4 has been amended to recite wherein the convex portion comprises a single discontinuous ring shape. Peng teaches a "plurality of concentric rings." Col. 4, Line 12. Admittedly, the concentric rings cited in Peng are discontinuous one with another. But if the plurality of concentric rings is the convex portion recited in claim 4, then the convex portion does not comprise a single discontinuous ring shape. Thus, claim 4 is in proper form for allowance based at least on its dependency from claim 1 and its own merits.

Claim 5 depends from claim 1. Claims 9 and 18 depend from claim 3. Claim 19 depends from claim 18. Claim 21 depends from claim 5. Thus, for at least the reasons mentioned above with respect to claims 1 and 3, claims 5, 9, 18-19 and 21 are in proper form for allowance.

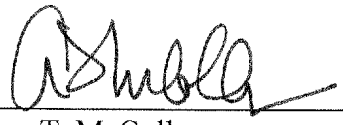
Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi and Cho as applied to claim 19 supra, and further in combination with Yunus (2003/0234447). Claim 20 has been cancelled.

Claim 19 has been amended to include the word "of" between the words "method" and "claim."

For the foregoing reasons, reconsideration and allowance of claims 1, 3-5, 7, 9, 10, 12, 17-19 and 21 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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